IN THE CLAIMS

Claim 1 (currently amended): An integrated circuit comprising:

an output buffer receiving a first value followed by a second value, wherein said first value is not equal to said second value; ~~and~~

<u>a voltage adjusting block to determine a total strength to be applied to said output buffer; and</u>

a control block changing a strength of said output buffer gradually while said output buffer provides said second value as a buffer output <u>to reach said total strength</u>.

Claim 2 (original): The integrated circuit of claim 1, wherein said output buffer comprises a drive transistor, and wherein said control block comprises:

a capacitor provided at a gate terminal of said drive transistor; and

a current source for altering the total charge on said capacitor slowly to change said strength gradually.

Claim 3 (original): The integrated circuit of claim 2, wherein said capacitor comprises a gate capacitance of said drive transistor.

Claim 4 (original): The integrated circuit of claim 2, wherein said output buffer comprises a plurality of inverters, wherein one of said plurality of inverters comprises said drive transistor.

Claim 5 (original): The integrated circuit of claim 4, wherein said drive transistor is contained in a last one of said plurality of inverters.

Claim 6 (original): The integrated circuit of claim 2, wherein said drive transistor comprises a PMOS transistor, wherein said current source discharges said capacitor to control said drive strength when said second value is greater than said first value.

Claim 7 (currently amended): The integrated circuit of claim 6, wherein said control block comprises:

a voltage adjusting block which determines ~~a~~ the total strength to be applied to said drive transistor when said second value is greater than said first value, and provides a PCTRL signal representing said total strength; and

a slew controller block coupled to said drive transistor, said slew controller block containing said current source, wherein said current source receives said PCTRL to determine the amount of current to supply to discharge said capacitor.

Claim 8 (original): The integrated circuit of claim 7, wherein said control block comprises:

a delay module delaying a clock signal to generate a delayed clock signal, wherein said clock signal is used to control the timing of reception of said first value and said second value; and

a comparator comparing said buffer output with a threshold voltage to determine whether said buffer output is rising at a desired rate, said comparator providing a comparison result,

wherein said voltage adjusting block adjusts said total strength according to said comparison result.

Claim 9 (original): The integrated circuit of claim 8, wherein said voltage adjusting block adjusts said total strength in multiple increments until said total strength equals a desired strength, wherein said desired strength is determined by said desired rate.

Claim 10 (original): The integrated circuit of claim 7, wherein said current source comprises:

a first transmission gate which conducts in one logical state of a clock signal and does not conduct on the other logical state of said clock signal, said first transmission gate being connected between a first node and a second node, said second node being coupled to a supply voltage;

a second transmission gate being connected between said first node and a third node, said second transmission gate conducting in said other logical state of said clock signal and not conducting in said one logical state of said clock signal, said third node being coupled to receive said PCTRL; and

a second capacitor coupled between said first node and said voltage supply, wherein a desired amount of current to discharge said capacitor is generated at said third node.

Claim 11 (original): The integrated circuit of claim 10, wherein the capacitance of said second capacitor equals the capacitance of said capacitor.

Claim 12 (original): The integrated circuit of claim 11, wherein said current source further comprises a drop transistor connected between said supply voltage and said second node, said drop transistor providing a voltage drop to apply a voltage of said supply voltage less said voltage drop at said second node so as to switch off said drive transistor.

Claim 13 (original): The integrated circuit of claim 12, further comprising:

a second drop transistor provided between said supply voltage and a gate terminal of said PMOS transistor, wherein said second drop transistor also provides said voltage drop to apply a voltage of said supply voltage less said voltage drop at said gate terminal of said PMOS transistor.

Claim 14 (original): The integrated circuit of claim 13, further comprising a clamping circuit to clamp the voltage at the gate terminal of said PMOS transistor to said PCTRL.

Claim 15 (original): The integrated circuit of claim 2, wherein said drive transistor comprises a NMOS transistor, wherein said current source charges said capacitor to control said drive strength when said second value is less than said first value.

Claim 16 (original): The integrated circuit of claim 6, wherein said control block comprises:

a voltage adjusting block which determines a total strength to be applied to said drive transistor when said second value is less than said first value, and provides a NCTRL signal representing said total strength; and

a slew controller block coupled to said drive transistor, said slew controller block containing said current source, wherein said current source receives said NCTRL to determine the amount of current to supply to discharge said capacitor.

Claim 17 (original): The integrated circuit of claim 16, wherein said control block comprises:

a delay module delaying a clock signal to generate a delayed clock signal, wherein said clock signal is used to control the timing of reception of said first value and said second value; and

a comparator comparing said buffer output with a threshold voltage to determine whether said buffer output is falling at a desired rate, said comparator providing a comparison result,

wherein said voltage adjusting block adjusts said total strength according to said comparison result.

Claim 18 (original): The integrated circuit of claim 13, further comprising a clamping circuit to clamp the voltage at the gate terminal of said NMOS transistor to said NCTRL.

Claim 19 (currently amended): The integrated circuit of claim 1, wherein said strength is changed such that an output signal of said output buffer changes from a first voltage level representing said first value to a second voltage level representing said second value in a duration which is substantially more than 15% of a clock cycle duration ~~using which said first value and said second value are received~~.

Claim 20 (currently amended): The integrated circuit of claim ~~1~~ 19, wherein said duration equals at least 40% of said clock cycle duration.

Claim 21 (currently amended): A device comprising:

an output buffer receiving a first value followed by a second value, wherein said first value is not equal to said second value; ~~and~~

a voltage adjusting block to determine a total strength applied to said output buffer; and

a control block changing a strength of said output buffer gradually while said output buffer provides said second value as a buffer output to reach said total strength.

Claim 22 (original): The device of claim 21, wherein said output buffer comprises a drive transistor, and wherein said control block comprises:

a capacitor provided at a gate terminal of said drive transistor;

a current source for altering the total charge on said capacitor slowly to change said strength gradually.

Claim 23 (original): The device of claim 22, wherein said capacitor comprises a gate capacitance of said drive transistor.

Claim 24 (original): The device of claim 22, wherein said output buffer comprises a plurality of inverters, wherein one of said plurality of inverters comprises said drive transistor.

Claim 25 (original): The device of claim 24, wherein said drive transistor is contained in a last one of said plurality of inverters.

Claim 26 (original): The device of claim 22, wherein said drive transistor comprises a PMOS transistor, wherein said current source discharges said capacitor to control said drive strength when said second value is greater than said first value.

Claim 27 (original): The device of claim 26, wherein said control block comprises:

a voltage adjusting block which determines a total strength to be applied to said drive transistor when said second value is greater than said first value, and provides a PCTRL signal representing said total strength; and

a slew controller block coupled to said drive transistor, said slew controller block containing said current source, wherein said current source receives said PCTRL to determine the amount of current to supply to discharge said capacitor.

Claim 28 (original): The device of claim 27, wherein said control block comprises:

a delay module delaying a clock signal to generate a delayed clock signal, wherein said clock signal is used to control the timing of reception of said first value and said second value; and

a comparator comparing said buffer output with a threshold voltage to determine whether said buffer output is rising at a desired rate, said comparator providing a comparison result,

wherein said voltage adjusting block adjusts said total strength according to said comparison result.

Claim 29 (original): The device of claim 28, wherein said voltage adjusting block adjusts said total strength in multiple increments until said total strength equals a desired strength, wherein said desired strength is determined by said desired rate.

Claim 30 (original): The device of claim 27, wherein said current source comprises:

a first transmission gate which conducts in one logical state of a clock signal and does not conduct on the other logical state of said clock signal, said first transmission gate being connected between a first node and a second node, said second node being coupled to a supply voltage;

a second transmission gate being connected between said first node and a third node, said second transmission gate conducting in said other logical state of said clock signal and not conducting in said one logical state of said clock signal, said third node being coupled to receive said PCTRL; and

a second capacitor coupled between said first node and said voltage supply, wherein a desired amount of current to discharge said capacitor is generated at said third node.

Claim 31 (original): The device of claim 30, wherein the capacitance of said second capacitor equals the capacitance of said capacitor.

Claim 32 (original): The device of claim 31, wherein said current source further comprises a drop transistor connected between said supply voltage and said second node, said drop transistor providing a voltage drop to apply a voltage of said supply voltage less said voltage drop at said second node.

Claim 33 (original): The device of claim 32, further comprising:

a second drop transistor provided between said supply voltage and a gate terminal of said PMOS transistor, wherein said second drop transistor also provides said voltage drop to apply a voltage of said supply voltage less said voltage drop at said gate terminal of said PMOS transistor.

Claim 34 (original): The device of claim 33, further comprising a clamping circuit to clamp the voltage at the gate terminal of said PMOS transistor to said PCTRL.

Claim 35 (original): The device of claim 22, wherein said drive transistor comprises a NMOS transistor, wherein said current source charges said capacitor to control said drive strength when said second value is less than said first value.

Claim 36 (original): The device of claim 26, wherein said control block comprises:

a voltage adjusting block which determines a total strength to be applied to said drive transistor when said second value is less than said first value, and provides a NCTRL signal representing said total strength; and

a slew controller block coupled to said drive transistor, said slew controller block containing said current source, wherein said current source receives said NCTRL to determine the amount of current to supply to discharge said capacitor.

Claim 37 (original): The device of claim 36, wherein said control block comprises:

a delay module delaying a clock signal to generate a delayed clock signal, wherein said clock signal is used to control the timing of reception of said first value and said second value; and

a comparator comparing said buffer output with a threshold voltage to determine whether said buffer output is falling at a desired rate, said comparator providing a comparison result,

wherein said voltage adjusting block adjusts said total strength according to said comparison result.

Claim 38 (original): The device of claim 33, further comprising a clamping circuit to clamp the voltage at the gate terminal of said NMOS transistor to said NCTRL.

Claim 39 (currently amended): The device of claim 21, wherein said strength is changed such that an output signal of said output buffer changes from a first voltage level representing said first value to a second voltage level representing said second value in a duration which is substantially more than 15% of a clock cycle duration ~~using which said first value and said second value are received~~.

Claim 40 (currently amended): The device of claim ~~21~~ 39, wherein said duration equals at least 40% of said clock cycle duration.

Claim 41 (original): The device of claim 21, wherein said device further comprises a load receiving said buffer output.

Claim 42 (original): The device of claim 41, wherein said load comprises a transmission line.

Claim 43 (original): The device of claim 21, wherein said device comprises a wireless base station, said device further comprising:

an antenna receiving an external signal; and

an analog processor processing said external signal to generate said first value and said second value.

Claim 44 (currently amended): An apparatus comprising:

an output buffer receiving a transition from a first value to a second value, wherein said first value is not equal to said second value, said buffer providing said first value followed by said second value on a buffer output; ~~and~~

a voltage adjusting block to determine a total strength to be applied to said output buffer; and

means for changing a strength of said output buffer gradually while providing said second value on said buffer output to reach said total strength.

Claim 45 (original): The apparatus of claim 44, wherein said output buffer comprises an inverter containing a transistor, wherein said means for changing alters slowly an amount of charge on a capacitor provided at a gate terminal of said transistor.

Claim 46 (original): The apparatus of claim 45, wherein said capacitor comprises a gate capacitance of said gate terminal.

Claim 47 (original): The apparatus of claim 45, wherein said means for changing comprises a current source to perform said altering.

Claim 48 (currently amended): A method of processing a transition from a first value to a second value, wherein said first value is not equal to said second value, said method comprising:

receiving said first value followed by said second value on a buffer input of an output buffer;

providing said first value on a buffer output of said output buffer; ~~and~~

<u>determining a total strength of said output buffer; and</u>

changing a strength of said output buffer gradually while providing said second value on said buffer output <u>to reach said total strength</u>.

Claim 49 (original): The method of claim 48, wherein said output buffer comprises an inverter containing a transistor, said changing comprises altering slowly an amount of charge on a capacitor provided at a gate terminal of said transistor.

Claim 50 (original): The method of claim 49, wherein said capacitor comprises a gate capacitance of said gate terminal.

Claim 51 (original): The method of claim 49, wherein said changing is performed using a current source.

Claim 52 (original): The method of claim 51, wherein said strength is changed such that an output signal of said output buffer changes from a first voltage level representing said first value to a second voltage level representing said second value in a duration which is substantially more than 15% of a clock cycle duration using which said first value and said second value are received.

Claim 53 (original): The method of claim 52, wherein said duration equals at least 40% of said clock cycle duration.